Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

Claim 1 (currently amended): A MOS transistor in a single-transistor memory cell, comprising:

a semiconductor substrate having a substrate surface, a first conductive region and a second conductive region;

a gate oxide disposed on said substrate surface;

a gate disposed on said gate oxide over an area between said first conductive region and said second conductive region and having ~~at least one~~ side ~~wall~~ walls adjacent ~~at least one~~ respective ones of said conductive regions;

a silicon oxide passivation layer disposed on said side wall of said gate; and

an insulating silicon nitride spacer disposed on said silicon oxide passivation layer, said spacer acting as an oxidation barrier;

said gate oxide insulating said gate from said semiconductor substrate and having a thickened area in a region below at least one of said side ~~wall~~ walls ~~of said gate and~~ adjacent said conductive regions.

Claim 2 (cancelled).

Claim 3 (previously presented): The MOS transistor according to claim 1, wherein said gate includes a layer selected from the group consisting of a tungsten silicide layer and a polysilicon layer.

Claim 4 (previously presented): The MOS transistor according to claim 1, wherein said gate includes a tungsten silicide layer and a polysilicon layer.

Claim 5 (original): The MOS transistor according to claim 1, wherein said gate includes a layer selected from the group consisting of a tungsten silicide layer and a polysilicon layer.

Claim 6 (original): The MOS transistor according to claim 1, wherein said gate includes a tungsten silicide layer and a polysilicon layer.

Claim 7 (original): A selection transistor in a DRAM memory cell, comprising the MOS transistor according to claim 6.

Claim 8 (original): A selection transistor in a DRAM memory cell, comprising the MOS transistor according to claim 1.